ABSTRACT

[0040] A resistive cross point array memory device comprising a plurality of word lines extending in a row direction, a plurality of bit lines extending in a column direction such that a plurality of cross points is formed at intersections between the word and bit lines, and at least one memory element formed in at least one of the cross points. The memory element comprises a first tunnel junction having a bottom conductor, a top conductor, a barrier layer adjacent the bottom conductor, and wherein the bottom conductor comprises a non-uniform upper surface.